A Low-Noise CMOS SPAD Pixel With 12.1 Ps SPTR and 3 Ns Dead Time

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Abstract—Single-photon avalanche diodes (SPADs) have become the sensor of choice in many applications whenever high sensitivity, low noise, and sharp timing performance are required, simultaneously. Recently, SPADs designed in CMOS technology, have yielded moderately good performance in these parameters, but never equaling their counterparts fabricated in highly customized, non-standard technologies. The arguments in favor of CMOS-compatible SPADs were miniaturization, cost and scalability. In this paper, we present the first CMOS SPAD with performance comparable or better than that of the best custom SPADs, to date. The SPAD-based design, fully integrated in 180 nm CMOS technology, achieves a peak photon detection probability (PDP) of 55% ± 480 nm with a very broad spectrum spanning from near ultraviolet (NUV) to near infrared (NIR) and a normalized dark count rate (DCR) of 0.2 cps/µm², both at 6 V of excess bias. Thanks to a dedicated CMOS pixel circuit front-end, an afterpulsing probability of about 0.1% at a dead time of 3 ns were achieved. We designed three SPADs with a diameter of 25, 50, and 100 µm to study the impact of size on the timing jitter and to create a scaling law for SPADs. For these SPADs, a single-photon time resolution (SPTR) of 12.1 ps, 16 ps, and 27 ps (FWHM) was achieved at 6 V of excess bias, respectively. The SPADs operate in a wide range of temperatures, from −65 ◦C to 40 ◦C, reaching a normalized DCR of 1.6 mcps/µm² at 6 V of excess bias for the 25 µm SPAD at −65 ◦C. The proposed SPADs are ideal for a wide range of applications, including (quantum) LIDAR, super-resolution microscopy, quantum random number generators, quantum key distribution, fluorescence lifetime imaging, time-resolved Raman spectroscopy, to name a few. All these applications can take advantage of the vastly improved performance of our detectors, while enjoying the opportunities of megapixel resolutions promised by the economy of scale that is offered by CMOS technologies.

Index Terms—Active reset, cascode, jitter, low noise, low power, photon detection probability (PDP), pixel, quantum key distribution (QKD), single-photon avalanche diode (SPAD), timing.

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Fig. 1. Micrograph of the implemented chip 1 (top), chip 2 (middle), and chip 3 (bottom) with a zoom-in on the SPAD pixel (top-right of each image). These devices embed four SPADs of 25 µm, 50 µm, and 100 µm for chip 1, 2, and 3 respectively. Each SPAD has a dedicated pixel and a pixel pitch of 250 µm.

controllability and observability of the system, each chip has a large padring. Several pads were added in this prototyping phase to ensure the possibility of fine tuning the several control voltages of the pixel circuit, together with the high voltage to bias the SPAD, digital VDD, ground, and ESD supplies. The SPADs, implemented in 180 nm CMOS technology, rely on a p-i-n structure, similar to [21]. Fig. 2 shows the cross-section of the SPAD (top) and a TCAD simulation of the electric field in 2D, as well as a quantitative plot of the field along the vertical axis. The SPAD is a substrate-isolated type, where a p-well (PW) layer forms the anode of the SPAD and a buried n-well (BNW) layer creates the cathode contact. The latter is connected to the high voltage through a deep-n-well (DNW). An epi layer between anode and cathode allows a fairly large high-field region (Fig. 2, bottom), thus achieving a large sensitivity spectrum. The simulation results correspond to the SPAD operation at an excess bias voltage of 6 V.

The SPAD breakdown voltage was measured to be about 22 V at room temperature. The corresponding I-V curve is shown in Fig. 3 under both dark and illuminated conditions.

The SPAD front-end circuit, shown in Fig. 4, was inspired by [33], whereas cascode transistor $M_1$ is used as a resistive divider, along with $M_2$ to enable high excess bias (up to 11 V) [34] in combination with thin-oxide MOS transistors in the remainder of the front-end.

The gate of $M_1$ is fixed at $V_{CAS}$, supplied externally. When an avalanche is triggered in the SPAD, the voltage at the source of $M_1$ rises, thus decreasing the transistor overdrive. When the voltage reaches $V_{CAS} - V_{th}$, $M_1$ turns off boosting the impedance seen at the SPAD’s anode. Thanks to the body effect acting on these transistors, the overdrive of $M_1$ is dynamically reduced, thus making it turn off faster.
Both passive and active recharge strategies are available in the pixel and can be used independently. $M_5$, controlled by $V_{pq}$, is used to disable the passive quenching/recharge branch, represented by $M_3$. Active recharge is formed by $M_2$ and $M_3$, the latter being turned on by the feedback loop represented by the OR gate, Schmitt trigger, and tunable delay element. The loop acts as a programmable-length monostable. The delay element is implemented using a current starved inverter (CSI) with a series voltage controlled transistor for both pMOS and nMOS branches (Fig. 4 right). Controlling this delay, and thus the hold-off time is important to control afterpulsing, especially in relatively large SPADs. This mechanism determines both the pulse width at the output and, in large part, the dead time. To guarantee the stability of the monostable and to get sharp edges at the output, an inverting Schmitt trigger was added, while, to improve the linearity of the CSI controls, a current mirror was included [35]. The slew rate of the output was maximized, unlike in [34], using a custom buffering chain to the bonding pad. This solution ensured an output slew rate of approximately 1 V/ns.

### III. Noise Performance

#### A. Dark Count Rate

Dark count rate (DCR) was measured at different excess bias voltages for all three SPAD structures (Fig. 5). The measurement was performed at room temperature using an oscilloscope (Teledyne LeCroy WaveMaster 813 Zi-B). To a first approximation, DCR is linear in the area of the active region. However, a super-linear behavior is generally observed in the normalized median DCR on the active area reaches a value of 4 mcps/$\mu$m at $8 V_{ex}$ for a diameter of 25 $\mu$m, operating at $-65 ^\circ C$. The normalized DCR decreases by about three orders of magnitude, reaching a value of 1.6 mcps/$\mu$m$^2$ at $6 V_{ex}$ for a diameter of 25 $\mu$m, operating at $-65 ^\circ C$. The normalized DCR decreases by about three orders of magnitude, reaching a value of 1.6 mcps/$\mu$m$^2$ at $6 V_{ex}$ for a diameter of 25 $\mu$m, operating at $-65 ^\circ C$.

#### B. Afterpulsing

Afterpulsing probability is another very important parameter, especially when one wants to minimize dead time through active recharge, so as to increase the maximum count rate in SPADs. This effect is due to some carriers, generated during the avalanche process, that may be captured by deep-level traps [36]–[38]. These carriers are then released after a statistical delay that depends on the lifetime of the traps [37], [38]. If a free carrier is released in a region where the electric field is sufficiently high it can ignite another avalanche. In general, the probability that this event occurs is more frequent with short dead times. Afterpulsing characterization for silicon SPADs is performed by histogramming the pulse inter-arrival time. This can be measured in the dark or under dim and uniform illumination. It can also be indirectly obtained by estimating the lifetime and density of traps using the time-correlated carriers counting (TCCC) technique [38], [39], which is typically more useful for III-V SPADs where the afterpulsing probability is significantly higher. In the presented work, the afterpulsing probability was obtained through inter-arrival histogramming under controlled dim illumination. Fig. 7 shows the measured inter-arrival time between pulses generated by the 25-$\mu$m SPAD at $6 V_{ex}$. The SPAD dead time was set at about 11 ns using the integrated active recharge circuit described earlier.

In Fig. 8 it is possible to see the measured afterpulsing probability on the same SPAD, as a function of the pulse width. The afterpulsing probability remains as low as 0.1% for a pulse width of about 5 ns. With the current architecture, the minimum achievable SPAD dead time is 3 ns.
Fig. 6. Top: DCR measured at different temperatures; Middle: DCR shown as a function of the excess bias voltage; Bottom: Breakdown voltage as a function of temperature. The results refer to a SPAD diameter of 25 µm (left side) and 100 µm (right side), respectively.

IV. SENSITIVITY PERFORMANCE

A. PDP Setup

The most common method of measuring the PDP is to create an area with uniform photon flux of a particular wavelength and compare the responsivity of the SPAD under test to a calibrated reference device (usually a photodiode). The setup used to measure PDP is based on the continuous light technique [40], schematically shown in Fig. 9. The setup comprises a wide-spectrum Xenon lamp that generates wide spectrum light, a monochromator, an integrating sphere, a calibrated reference photodiode (PD) with a precision source and measurement unit (SMU) to measure the photocurrent generated by the PD, and a universal counter connected to the device under test (DUT). The integrating sphere and the DUT are enclosed in a light tight box to eliminate any source of background noise that would affect the measurement. A custom software was developed to automate the scan at a very fine wavelength resolution. The DUT has been placed at distance \( L \) from the output window of the integrating sphere, so as to ensure lower light level and high uniformity [41]. The reason to have a lower light level is that the SPAD (sensible to single photons) can be saturated if exposed to high light level, thus causing pile-up, which distorts the SPAD’s sensitivity curve, causing an underestimation of PDP. Moreover, a stronger light impinging on the reference photodiode can improve its SNR. A 45 s integration time was used for each step. For each value of excess bias, the DCR is measured before starting the acquisition under the light. This value is then used to compute
Fig. 7. Inter arrival time distribution measured with the pulse width of 11 ns on the SPAD of 25 μm size. The measurement is taken at a temperature of 25 °C.

Fig. 8. Afterpulsing probability as a function of the pulse width on the 25 μm diameter and 100 μm diameter SPADs at 6 V excess bias. All the measurements are taken at a temperature of 25 °C.

the PDP as shown in [40]:

\[ PDP(\lambda) = \eta \frac{S - DCR}{A_{SPAD} F_{PD}(\lambda)} = \eta \frac{F_{SPAD}(\lambda)}{F_{PD}(\lambda)} \] (1)

Where \( \eta \) is a light ratio computed during the calibration phase measuring the light power at the integrating sphere output port and at the location of the DUT with a calibrated reference photodiode; \( S \) is the number of pulses at the SPAD output when exposed to light; \( A_{SPAD} \) is the active area of the SPAD; \( F_{PD}(\lambda) \) is the photon flux detected by the reference photodiode.

B. PDP Results

The PDP is plotted in Fig. 10 as a function of wavelength (top) and excess bias voltage (bottom). All the measurements were performed at room temperature. The wavelength scan was performed with a step of 10 nm. The sensitivity peak is 55% at 480 nm at 6 V \( V_{ex} \). These results are consistent with [21], [34] for similar SPAD cross-sections. The relatively large sensitivity spectrum is also in line with the structure used (Fig. 2). Note the typical PDP saturation above 5 V \( V_{ex} \). At and above this voltage, the PDP becomes increasingly insensitive to variations of breakdown voltage, which makes this SPAD amenable to integration in large arrays, where the breakdown voltage could vary significantly across the chip, thereby causing unwanted PDP variability.

V. TIMING JITTER

A. Jitter Setup

The setup used to evaluate timing jitter in the DUT shown in Fig. 11 is based on [42]. The setup comprises a femtosecond
laser (Amplitude Systèmes SA, S-Pulse HR SP), capable of generating 150 fs pulses at a wavelength of 1030 nm and 515 nm after second-harmonic generation (SHG). A fast photodiode (Newport InGaAs Photodetector, 45 GHz bandwidth) is used as a timing reference, while the upconverted beam is attenuated by a bank of neutral density filters (NDFs), so as to achieve single-photon detection regime. The DUT has a high-impedance output and thus an active probe is used to capture the output. An oscilloscope (LeCroy WaveMaster 813 Zi-B) is used to capture both the waveform from the DUT and the reference PD.

B. Jitter Results

Timing jitter measurements for the 3 device sizes are shown in Fig. 12. The plot shows the histograms of the response of the SPADs when biased at an excess bias voltage of 6 V and at room temperature. The oscilloscope trigger threshold was set at 400 mV for the SPAD pulse and 300 mV for the PD. The laser repetition rate is 100 MHz and the light was reduced in order to detect less than a laser pulse every 100. The jitter value (FWHM) of the response distribution was measured at 12.1 ps for a diameter of 25 μm, 16 ps for 50 μm, and 27.2 ps for 100 μm. To capture the diffusion tails, the full width at tenth of maximum (FWTM) was extracted as well; it results in 55.7 ps for a diameter of 25 μm, 66.8 ps for 50 μm, and 91.7 ps for 100 μm. The exponential time constant for the diffusion tails was also extracted from the plot to be 31.5 ps, 40.7 ps and 38 ps for the 25, 50 and 100 μm SPAD, respectively.

The plots in Fig. 13 show the response of a 100 μm SPAD with two excess bias voltages of 6 and 8 V, with an improvement of the jitter from 27.2 to 23.5 ps FWHM. Also in this case the exponential time constant of the diffusion tail was extracted and it is 38 ps for 6 V excess bias and 33.1 ps for 8 V excess bias.

It is important to note that these results were obtained without the need for low threshold comparators, thus a simplified circuit can be used in each pixel, thereby ensuring scalability to large arrays of pixels.

VI. DISCUSSION

Table I and Fig. 14 summarize the performance of several state-of-the-art devices found in the literature in comparison to the SPADs presented in this work. Many of the SPADs listed here were developed in standard technologies. SPADs implemented in older technology nodes (between 0.35 μm and
TABLE I
SUMMARY OF SPAD PERFORMANCE

<table>
<thead>
<tr>
<th>Technology</th>
<th>Diameter (µm)</th>
<th>( V_{E X} / V_{TH} ) (V)</th>
<th>Peak PDP (%) @ λ (nm)</th>
<th>PDP (%) @ 850 nm</th>
<th>DCR/unit area (cps/µm²)</th>
<th>AP (%)</th>
<th>Jitter (ps)</th>
<th>PoM ( \gamma )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ghioni [7]</td>
<td>Custom Thin</td>
<td>50-200</td>
<td>5-10/30-35</td>
<td>32-68 @ 350</td>
<td>12-15</td>
<td>0.4-1.6³</td>
<td>²</td>
<td>35²</td>
</tr>
<tr>
<td>Guarnieri [8]</td>
<td>Custom RE</td>
<td>50</td>
<td>20/45-55</td>
<td>58 @ 650</td>
<td>28</td>
<td>0.3³</td>
<td>3°</td>
<td>N/A</td>
</tr>
<tr>
<td>Villa [16]</td>
<td>350</td>
<td>10-500</td>
<td>5-20/65</td>
<td>37-55 @ 450</td>
<td>2.45</td>
<td>0.05⁵</td>
<td>1°</td>
<td>90²</td>
</tr>
<tr>
<td>Leitner [17]</td>
<td>180</td>
<td>10</td>
<td>1.3-3.21</td>
<td>35-47 @ 450</td>
<td>N/A⁹</td>
<td>0.3-1.8²</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Veerapan [18]</td>
<td>180</td>
<td>12</td>
<td>2-10/23.5</td>
<td>24-48 @ 480</td>
<td>3-8</td>
<td>0.16-176⁴</td>
<td>0.03-0.3³</td>
<td>112-88³</td>
</tr>
<tr>
<td>Veerapan [19]</td>
<td>180</td>
<td>12</td>
<td>1.4/14</td>
<td>23-47 @ 480</td>
<td>4.7</td>
<td>0.28-16⁴</td>
<td>0.2²</td>
<td>161-14³</td>
</tr>
<tr>
<td>Veerapan [21]</td>
<td>180</td>
<td>12</td>
<td>1-12/25</td>
<td>18-47 @ 620</td>
<td>2.8</td>
<td>0.2-6²</td>
<td>7.2²</td>
<td>190-10²</td>
</tr>
<tr>
<td>Xu [22]</td>
<td>150</td>
<td>10</td>
<td>3-5/19</td>
<td>24-33 @ 450</td>
<td>3-7.5</td>
<td>0.1-1</td>
<td>1.1-3</td>
<td>42²</td>
</tr>
<tr>
<td>Lee [20]</td>
<td>140(200)</td>
<td>12</td>
<td>0.5-3.11</td>
<td>23-65 @ 450</td>
<td>2.5-9.6</td>
<td>0.29-6.7</td>
<td>1.7⁶</td>
<td>65⁶</td>
</tr>
<tr>
<td>Richardson [13]</td>
<td>130</td>
<td>8</td>
<td>0.6-1.4/14</td>
<td>18-28 @ 500</td>
<td>3.5</td>
<td>0.24-0.6³</td>
<td>0.02⁶</td>
<td>200⁶</td>
</tr>
<tr>
<td>Richardson [12]</td>
<td>130</td>
<td>8</td>
<td>0.2-1.2/12-13</td>
<td>18-33 @ 450</td>
<td>3.5</td>
<td>0.4-0.8</td>
<td>0.02⁶</td>
<td>237-11⁶</td>
</tr>
<tr>
<td>Nicolosi [10]</td>
<td>130</td>
<td>10</td>
<td>1.3-5/10</td>
<td>31-41 @ 450</td>
<td>3</td>
<td>120-130³</td>
<td>N/A⁴</td>
<td>N/A</td>
</tr>
<tr>
<td>Nicolosi [43]</td>
<td>180</td>
<td>25</td>
<td>5.2/0.5</td>
<td>64.8 @ 610¹⁴</td>
<td>24</td>
<td>0.6</td>
<td>0.49³⁶</td>
<td>190</td>
</tr>
<tr>
<td>Gersbach [11]</td>
<td>130</td>
<td>4.3</td>
<td>1-2/9</td>
<td>18-30 @ 480</td>
<td>3.5-5</td>
<td>1.5-11.5</td>
<td>1²</td>
<td>125²</td>
</tr>
<tr>
<td>Chabot [15]</td>
<td>65</td>
<td>8</td>
<td>0.05-0.4/0.9</td>
<td>2-5.5 @ 420</td>
<td>0.2-0.4</td>
<td>340-15³</td>
<td>6²</td>
<td>1²</td>
</tr>
<tr>
<td>Sanzaro(A) [24]</td>
<td>160(BCD)</td>
<td>10-40</td>
<td>3-9/36</td>
<td>31-38 @ 450</td>
<td>2.5-6.5</td>
<td>0.12-0.2²</td>
<td>0.49-3.5²</td>
<td>39-2⁶</td>
</tr>
<tr>
<td>Sanzaro(B) [24]</td>
<td>160(BCD)</td>
<td>10-40</td>
<td>3-9/25</td>
<td>2.47 @ 450</td>
<td>2.5-6.5</td>
<td>0.1-0.1³</td>
<td>0.02-0.14³</td>
<td>36-2⁶</td>
</tr>
<tr>
<td>Sanzaro(C) [24]</td>
<td>160(BCD)</td>
<td>10-40</td>
<td>3-9/26</td>
<td>55-71 @ 490</td>
<td>6-9</td>
<td>0.13-0.19³</td>
<td>0.41-1.2⁶</td>
<td>41-2³</td>
</tr>
<tr>
<td>Pellegrini [25]</td>
<td>40</td>
<td>18.36</td>
<td>1/3/5</td>
<td>48 @ 460⁹</td>
<td>5</td>
<td>N/A³</td>
<td>10¹</td>
<td>N/A</td>
</tr>
<tr>
<td>Nolet [5]</td>
<td>65</td>
<td>20</td>
<td>1.75-5.9</td>
<td>8 @ 470</td>
<td>N/A</td>
<td>2.8k</td>
<td>&lt;10²</td>
<td>78⁵</td>
</tr>
<tr>
<td>Webster [14]</td>
<td>90</td>
<td>4.9</td>
<td>14.5/29.2</td>
<td>74 @ 700</td>
<td>22</td>
<td>8.1k</td>
<td>0.37⁵</td>
<td>84¹</td>
</tr>
</tbody>
</table>

⁴ At 20°C, ¹ 200 µm diameter, at 25°C, 80 ns dead time, \( V_{E X} = 5 \) V, 820 nm wavelength. ² At 25°C, 30 µm diameter, at 25°C, 40 ns dead time, \( V_{E X} = 5 \) V, integrated AQC. ³ A time resolution of 28-37 ps FWHM and a diffusion tail of 160-340 ps were demonstrated in Ref. [45] using the substrate bias as a trade-off parameter between jitter and diffusion tail. ⁴ PDE = 10-13% at 800 nm. ⁵ Substrate not isolated SPAD. ⁶ 30 µm diameter, at 25°C, 40 ns dead time, \( V_{E X} = 4 \) V, 8.300 ns dead time, \( V_{E X} = 2-10 \) V, 637 nm wavelength. ⁷ Integrated AQC. ⁸ 30 µm diameter, at 25°C, 40 ns dead time, \( V_{E X} = 2 \) V, 405 nm wavelength. ⁹ 300 ns dead time, \( V_{E X} = 2 \) V. ¹⁰ 815 nm wavelength. ¹¹ For a dead time of 3 ns on the 25 µm-diameter and 100 µm-diameter SPADs at 25°C and 6 V excess bias. ¹² 5 µs dead time. ¹³ Measured between 1 V and 6 V excess bias at 25°C. ¹⁴ 25 µm diameter, at 20°C with an excess bias of 6 V. ¹⁵ Value taken at 1 V and 6 V excess bias.

Fig. 14. Left: visualization of state-of-the-art performance in terms of PDP and timing jitter. The best solutions are located toward the top-left corner of the graph. Right: Performance comparison in terms of normalized DCR and timing jitter. The best performance is found at the bottom-left corner of the graph.

0.16 µm) exhibit the best sensitivity performance [16]–[19], [21], [24]. Instead, in more recent nodes, where higher doping and shallower standard layers are used, peak PDP does not usually exceed 32% and noise is higher [10]–[13], [15], [20], [22]. In [43] it is shown how very high PDPs can be achieved in the red in a 180 nm CMOS node using custom layers. However, this SPAD is not isolated, and thus the integration of front-end circuits is not straightforward. In addition, the achieved timing jitter is high because of its large drift region.

The PDP performance of the devices presented in this work is among the best ever reported in the literature for substrate isolated SPADs. The peak value of ~54% at 480 nm with 5 V excess bias is quite close to that reported in [24], device (C), for the same bias. The noise performance reported in this work is also among the best shown in the literature (Fig. 14 right).

To the best of our knowledge, the timing jitter achieved in this work is superior to any other CMOS SPAD-based device reported in literature, except for [5], which reports a peak PDP of 8% and a DCR of 2800 cps/µm², while our device achieves a peak PDP of 55% and worst-case DCR of 0.23 cps/µm² (Fig. 14 left). Moreover, in our solution, we have shown the performance of the SPAD with a low-power digital front-end and without the need for any circuit that could affect power consumption, such as a low threshold comparators. Thus, we believe that the proposed SPAD is an example of a new generation of devices with similar or better performance than custom SPADs but allowing scalable...
architectures with little to no power budget restrictions. Finally, we believe that the reduction of the front-end circuit threshold could improve timing performance and power consumption even further.

VII. CONCLUSIONS

We report on the design and characterization of a new SPAD fabricated in 180 nm CMOS technology, exhibiting a performance comparable or better than that of the most advanced custom SPADs, to date. The devices have a peak PDP of 55% at 480 nm and DCR is as low as 0.2 cps/μm^2 at −65 °C, while the SPAD operated normally at 40 °C. The pixel circuit used allows the fine tuning of the SPAD dead time to control the maximum achievable count rate up to 300 Mcps, while afterpulsing remains in the order of 0.1%.

Three SPAD families were designed with 25, 50, and 100 μm. The SPTR reached 12.1 ps (FWHM) in the smallest SPAD and did not exceed 27 ps in the largest, all at 6 V of excess bias and room temperature. Low static power consumption is compatible with large arrays of SPADs, which makes this technology amenable to scalable Mpixel sensor architectures, suitable for a variety of applications demanding high sensitivity, low noise, and sharp timing performance.

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REFERENCES


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**Edoardo Charbon** (Fellow, IEEE) received the Diploma from ETH Zurich, the M.S. from the University of California at San Diego, and the Ph.D. from the University of California at Berkeley in 1988, 1991, and 1995, respectively, all in electrical engineering and EECS. He has consulted with numerous organizations, including Bosch, X-Fab, Texas Instruments, Maxim, Sony, Agilent, and the Carlyle Group. He was with Cadence Design Systems from 1995 to 2000, where he was the Architect of the company’s initiative on information hiding for intellectual property protection. In 2000, he joined Canesta Inc., as the Chief Architect, where he led the development of wireless 3-D CMOS image sensors. Since 2002 he has been a member of the faculty of EPFL. From 2008 to 2016 he was with Delft University of Technology’s as Chair of VLSI design. He has been the driving force behind the creation of deep-submicron CMOS SPAD technology, which is mass-produced since 2015 and is present in telemeters, proximity sensors, and medical diagnostics tools. His interests span from 3-D vision, LiDAR, FLIM, FCS, NIROT to super-resolution microscopy, time-resolved Raman spectroscopy, and cryo-CMOS circuits and systems for the control of qubit arrays in quantum computers. He has authored or co-authored over 400 papers and two books, and he holds 22 patents. Dr. Charbon is a Fellow of the Kavli Institute of Nanoscience Delft, a distinguished Lecturer of the IEEE, a visiting scholar of the W. M. Keck Institute for Space at Caltech, a Fellow of the Kavli Institute of Nanoscience Delft, a distinguished Lecturer of the IEEE Photonics Society, and a fellow of the IEEE.